PRODUCT/PROCESS CHANGE NOTIFICATION

PCN AMS/13/7827
Dated 22 Apr 2013

Wafer dimension change from 5 to 6 for HC1PA technology in ST Singapore

Table 1. Change Implementation Schedule

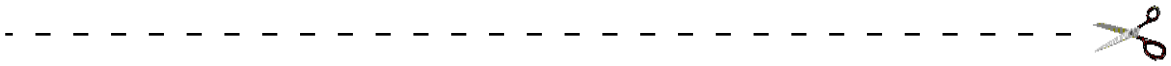
Forecasted implementation date for change	22-Apr-2013
Forecasted availability date of samples for customer	15-Apr-2013
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	15-Apr-2013
Estimated date of changed product first shipment	22-Jul-2013

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	see attached list
Type of change	Waferfab process change
Reason for change	To increase throughput by upgrading from 5 inches wafers to 6 inches wafers
Description of the change	Wafers sizes are upgraded from 5 inches to 6 inches, with electrical specifications of products remaining unchanged.
Change Product Identification	see datecode & lot number
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN AMS/13/7827**
Please sign and return to STMicroelectronics Sales Office	**Dated 22 Apr 2013**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

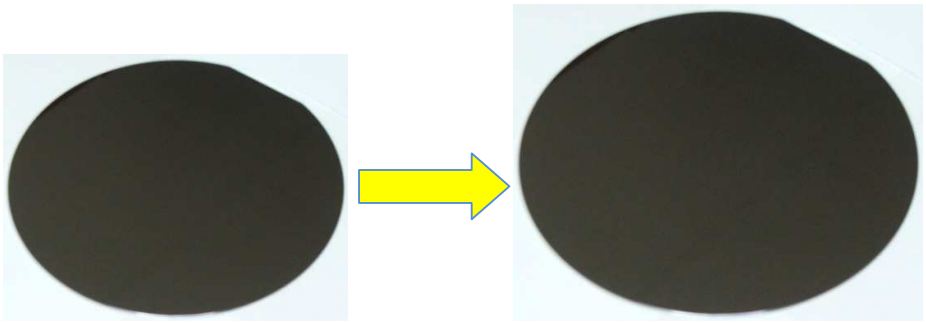
Name	Function
Camiolo, Jean	Marketing Manager
De marco, Alberto	Product Manager
Bugnard, Jean-Marc	Q.A. Manager

PRODUCT/PROCESS
CHANGE NOTIFICATION

PCN AMS/13/7827

Analog, MEMS and Sensor Group

Wafer dimension change from 5 inches to 6 inches for HC1PA technology in ST Singapore



5 inches 6 inches

HC1PA

WHAT:

Progressing on the activities related to HC1PA manufacturing processes, ST is glad to announce availability of 6 inches wafer production line, for AMS products.

Material	Current process 5 inches	Modified process 6 inches	Comment
diffusion location	ST Ang Mo Kio (Singapore) ST AMJ9	ST Ang Mo Kio (Singapore) ST AMJ9	No change
Wafer dimension	5 inches	6 inches	
OCR (Optical charac-ter recognition)	NO	YES	Laser marking on wafer, which allow better traceability
Metallization	AlSi	AlSi	No change
Passivation	Pvapox/Nitride	Pvapox/Nitride	No change
EWS	ST Singapore	ST Singapore	No change

For the complete list of part numbers affected by the change, please refer to the attached Product list.
Samples of test vehicles are available from week16 2013 and other samples upon customers request.

WHY:
To upgrade manufacturing line from 5 inches to 6 inches in order to improve customer service.

HOW:
The change that covers AMS (Analog, Mems & Sensors) products is qualified based on qualification plan here attached.
Here below you'll find the details of qualification plan.

Qualification program and results:

The qualification program consists mainly of comparative electrical characterization and reliability tests. Please refer to Reliability evaluation plan for all the details.

WHEN:
Production in ST Singapore in 6 inches for AMS is forecasted week17 2013 for HC1PA technology.

Marking and traceability:

Unless otherwise stated by customer specific requirement, the traceability of the parts assembled with the new material set will be ensured by datecode and lot number.

The changes here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all information reported on the relevant datasheets.
There is as well no change in the packing process or in the standard delivery quantities.

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change. After acknowledgement, lack of additional response within the 90 day period will constitute acceptance of the change (Jedec Standard No. 46-C).
In any case, first shipments may start earlier with customer's written agreement.

Change Qualification Plan

HC1PA transfer 5 to 6 inches

Test vehicle	
Product Lines:	*0912, 0914, 1930, 0372*
Product Families:	*Op amp / comparator*
P/Ns:	*TS912IYDT, TS914IYDT, TS393IYDT, TS372IDT*
Product Groups:	*AMS*
Product Divisions:	*Analog & Audio System*
Packages:	*SO8/SO14*
Silicon Process techn.:	*HC1PA*

Locations	
Wafer Diffusion Plants:	*ST Singapore*
EWS Plants:	*ST Singapore*
Assembly Plants:	*ST Bouskoura*
T&F Plants:	*ST Bouskoura*
Reliability Lab.:	*ST Grenoble*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Comment
1.0	05-Apr-2013	13	JM Bugnard	First issue

Reference document :

Note: This report is a summary of the qualification trials performed in good faith by STMicroelectronics in order to evaluate the potential qualification risks during the product life using a set of defined test methods.
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TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	Stress test qualification for automotive grade integrated circuits
AEC-Q101	Stress test qualification for automotive grade discrete semiconductors
AEC-Q001	Guidelines for part average testing
AEC-Q003	Guidelines for Characterizing the Electrical Performance of IC Products
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size

3 QUALIFICATION EVALUATION OVERVIEW

3.1 Objectives

Through this qualification plan, the HC1PA technology transfer is evaluated, to be diffused at ST Singapore in 6 inches instead of 5 inches.

3.2 Conclusion

Qualification Plan requirements must be fulfilled without exception. It is stressed that reliability tests must show that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests must demonstrate the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 CHANGE CHARACTERISTICS

4.1 Change description

Transfer of HC1PA technology from 5 inches to 6 inches.

4.2 Change details

Material	Current process 5 inches	Modified process 6 inches	Comment
diffusion location	ST Ang Mo Kio (Singapore) ST AMJ9	ST Ang Mo Kio (Singapore) ST AMJ9	No change
Wafer dimension	5 inches	6 inches	
OCR (Optical character recognition)	NO	YES	Laser marking on wafer, which allow better traceability
Metallization	AlSi	AlSi	No change
Passivation	Pvapox/Nitride	Pvapox/Nitride	No change
EWS	ST Singapore	ST Singapore	No change

4.3 Test vehicles description

	P/N *TS912IYDT*	P/N *TS914IYDT*	P/N *TS393IYDT*	P/N *TS372IDT*
Wafer/Die fab. information				
Wafer fab manufacturing location	ST Singapore	ST Singapore	ST Singapore	ST Singapore
Technology	HC1PA	HC1PA	HC1PA	HC1PA
Process family	CMOS	CMOS	CMOS	CMOS
Die finishing back side	Raw silicon	Raw silicon	Raw silicon	Raw silicon
Die size (microns)	2600x1950	4650x1960	1366x986	1540x1810
Bond pad metallization layers	AlSi	AlSi	AlSi	AlSi
Passivation type	Pvapox+Nitride	Pvapox+Nitride	Pvapox+Nitride	Pvapox+Nitride
Wafer Testing (EWS) information				
Electrical testing manufacturing location	ST Singapore	ST Singapore	ST Singapore	ST Singapore
Tester	ASL1000	ASL1000	ASL1000	ASL1000
Assembly information				
Assembly site	ST Bouskoura	ST Bouskoura	ST Bouskoura	ST Bouskoura
Package description	SO8	SO14	SO8	SO8
Molding compound	Sumitomo G700K	Sumitomo G700K	Sumitomo G700K	Sumitomo G700K
Frame material	Copper	Copper	Copper	Copper
Die attach process	Epoxy glue	Epoxy glue	Epoxy glue	Epoxy glue
Die attach material	Abklestick 8601-S25	Abklestick 8601-S25	Abklestick 8601-S25	Abklestick 8601-S25
Wire bonding process	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding
Wires bonding materials/diameters	Copper 1 mil	Copper 1 mil	Copper 1 mil	Copper 1 mil
Lead finishing process	Preplated frame	Preplated frame	Preplated frame	Preplated frame
Lead finishing/bump solder material	NiPdAgAu	NiPdAgAu	NiPdAgAu	NiPdAgAu
Final testing information				
Testing location	ST Bouskoura	ST Bouskoura	ST Bouskoura	ST Bouskoura
Tester	ASL1K	ASL1K	ASL1K	ASL1K

5 TESTS RESULTS SUMMARY

5.1 Test vehicles

Lot #	P/N	Process/ Package	Product Line	Comments
1	TS912IYDT	HC1PA/SO8	0912	
2	TS914IYDT	HC1PA/SO14	0914	
3	TS393IYDT	HC1PA/SO8	1930	Diffusion lot W247PXN
4	*TS372IDT*	HC1PA/SO8	0372	Diffusion lot W247PXL

5.2 Test plan and results summary

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS				Note
						Lot 1 0912	Lot 2 0914	Lot 3 1930	Lot4 0372	
Die Oriented Tests										
HTB High Temp. Bias	N	JESD22 A-108	Tj = 125°C, BIAS		168H 1000H	0/78 78			0/78 78	
ELFR Early Life Failure Rate	N	AEC Q100 - 008	Ta=125°C		48H	0/600	600	600	600	
Package oriented test										
PC Preconditioning		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Oven Reflow @ Tpeak=260°C 3 times		Final	PASS				
AC Auto Clave (Pressure Pot)	Y	JESD22 A-102	Pa=2Atm / Ta=121°C		168 H					
TC Temperature Cycling	Y	JESD22 A-104	Ta = -65°C to 150°C		100cy 500cy	0/78 0/78	78 78			
THB Temperature Humidity Bias	Y	JESD22 A-101	Ta = 85°C, RH = 85%, BIAS		168H 500 H					
Other Tests										
ESD Electro Static Discharge	-	AEC Q101-001, 002 and 005	HBM			3kV(0/3)	3	3	2kV(0/3)	
			CDM			1.5kV(0/3)	3	3	1.3kV(0/3)	
			MM			200V(0/3)	3	3	200V(0/3)	
LU Latchup			LU			0/6	6	6	0/6	

6 ANNEXES

6.1 Comparison Data Results

6.1.1 Electrical Data

Part Number: *TS393IYDT*

Table 4. $V_{CC}^+ = 5$ V, $V_{CC}^- = 0$ V, $T_{amb} = 25$ °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage(1) $V_{ic} = 2.5$ V, $V_{CC}^+ = 5$ V to 10 V $T_{min} \le T_{amb} \le T_{max}$		1.4	5 6.5	mV

Parameter	Results					
		Before Change		After Change		Note
test parameter	Unit	Avg	Cpk	Avg	Cpk	Note
Vio op amp A at 5V	mV	-1.30	>1.66	-1.54	>1.66	conform
Vio op amp B at 5V	mV	-1.19	>1.66	-1.41	>1.66	conform
Vio op amp A at 5V at Vic 3.5V	mV	-0.60	>2	-0.65	>2	conform
Vio op amp B at 5V at Vic 3.5V	mV	-0.53	>2	-0.54	>2	conform
Vio op amp A at 5V at Vic 1.5V	mV	-0.81	>2	-0.87	>2	conform
Vio op amp B at 5V at Vic 1.5V	mV	-0.72	>2	-0.75	>2	conform

Table 4. $V_{CC}^+ = 5$ V, $V_{CC}^- = 0$ V, $T_{amb} = 25$ °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{ib}	Input bias current(2) $V_{ic} = 2.5$ V $T_{min} \le T_{amb} \le T_{max}$		1	600	pA

Parameter	Results					
		Before Change		After Change		Note
test parameter	Unit	Avg	Cpk	Avg	Cpk	Note
Iibn at 5V op amp A	pA	-14.85	>2	-41.5	>2	conform
Iibn at 5V op amp B	pA	-17.9	>2	-61	>2	conform
Iibp at 5V op amp A	pA	-16.01	>2	-46.57	>2	conform
Iibp at 5V op amp B	pA	-19.45	>2	-45.71	>2	conform

Table 4. V_{CC}^+ = 5 V, V_{CC}^- = 0 V, T_{amb} = 25 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current (each comparator) No load - outputs low $T_{min} \le T_{amb} \le T_{max}$		10	20 25	µA

Parameter	Results					
		Before Change		After Change		
test parameter	Unit	Avg	Cpk	Avg	Cpk	Note
Icc 5V	mA	0.01	>2	0.01	>2	conform

Part Number: *TS372IDT*

Table 3. Electrical characteristics at V_{CC}+ = 5 V, V_{CC}- = 0 V, Tamb = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage (V_{ic} = $V_{icm\ min}$) (1) T_{amb} = 25°C $T_{min} \le T_{amb} \le T_{max}$		2	10 12	mV

Parameter	Results					
		Before Change		After Change		
test parameter	Unit	Avg	Cpk	Avg	Cpk	Note
Vio op amp A at 5V	mV	-0.1	>1.66	-1.0	>1.66	conform
Vio op amp B at 5V	mV	-0.4	>1.66	-1.0	>1.66	conform
Vio op amp A at 5V (Vic 2.5V)	mV	0.1	>1.66	-0.6	>1.66	conform
Vio op amp B at 5V (Vic 2.5V)	mV	0.0	>1.66	-0.7	>1.66	conform

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{ib}	Input offset current (2) T_{amb} = 25°C $T_{min} \le T_{amb} \le T_{max}$ TS372C TS372I/TS372M		1	150 300	pA

Parameter	Results					
		Before Change		After Change		
test parameter	Unit	Avg	Cpk	Avg	Cpk	Note
Iibn at 5V op amp A	pA	-40.0	>2	-93.2	>2	conform
Iibn at 5V op amp B	pA	-46.4	>2	-94.5	>2	conform
Iibp at 5V op amp A	pA	-51.9	>2	-34.6	>2	conform
Iibp at 5V op amp B	pA	-48.5	>2	-34.2	>2	conform

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current (each comparator) (V_{id} = 1 V, no load)		150	375	µA

Parameter	Results					
		Before Change		After Change		
test parameter	Unit	Avg	Cpk	Avg	Cpk	Note
Icc at 5V	mA	0.1	>2	0.1	>2	conform

Conclusion: New version in line with requirements.

Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operating Life **HTB** High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTRB High Temperature Reverse Bias **HTFB / HTGB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: • low power dissipation; • max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
ELFR Early Life Failure Rate	The device is stressed in biased conditions at the max junction temperature.	To evaluate the defects inducing failure in early life.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
THS Temperature Humidity Storage	The device is stored at controlled conditions of ambient temperature and relative humidity.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.

Test name	Description	Purpose
PTC Power & Temperature Cycling	The power and temperature cycling test is performed to determine the ability of a device to withstand alternate exposures at high and low temperature extremes with operating biases periodically applied and removed.	It is intended to simulate worst case conditions encountered in typical applications. Typical failure modes are related to parametric limits and functionality. Mechanical damage such as cracking, or breaking of the package will also be considered a failure provided such damage was not uinduced by fixturing or handling.
EV External Visual	Inspect device construction, marking and workmanship	To verify visual defects on device (form, marking,…).
LI Lead Integrity	Various tests allow determining the integrity lead/package interface and the lead itself when the lead(s) are bent due to faulty board assembly followed by rework of the part for reassembly.	This test is applicable to all throughhole devices and surface-mount devices requiring lead forming by the user.
WBP Wire Bond Pull	The wire is submitted to a pulling force (approximately normal to the surface of the die) able to achieve wire break or interface separation between ball/pad or stitch/lead.	To investigate and measure the integrity and robustness of the interface between wire and die or lead metallization
WBS Wire Bond Shear	The ball bond is submitted to a shear force (parallel to the pad area) able to cause the separation of the bonding surface between ball bond and pad area.	To investigate and measure the integrity and robustness of the bonding surface between ball bond and pad area.
DS Die Shear	This determination is based on a measure of force applied to the die, the type of failure resulting from this application of force (if failure occurs) and the visual appearance of the residual die attach media and substrate/header metallization.	The purpose of this test is to determine the integrity of materials and procedures used to attach semiconductor die or surface mounted passive elements to package headers or other substrates.
PD Physical Dimension	All physical dimension quoted in datasheet of the device are measured.	Verify physical dimensions to the applicable user device packaging specification for dimensions and tolerances.
SD Solderability	This evaluation is made on the basis of the ability of these terminations to be wetted and to produce a suitable fillet when coated by tin lead eutectic solder. A preconditioning test is included in this test method, which degrades the termination finish to provide a guard band against marginal finishes.	The purpose of this test method is to provide a referee condition for the evaluation of the solderability of terminations (including leads up to 0.125 inch in diameter) that will be assembled using tin lead eutectic solder. These procedures will test whether the packaging materials and processes used during the manufacturing operations process produce a component that can be successfully soldered to the next level assembly using tin lead eutectic solder.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. **CBM**: Charged Device Model **HBM**: Human Body Model **MM**: Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
LU Latch-Up	The device is submitted to a direct current forced/sunk into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effect inducing latch-up.

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